CREATIVE MICRO SYSTEMS
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9626

PRELIMINARY 9626 8K STATIC RANDOM ACCESS MEMORY (Note 3)

GENERAL DESCRIPTION: The 9626 is a fully static random access memory module specifically designed for compatibility with the M6800 Microprocessor Bus. It is pin and outline compatible with the Motorola EXORciser* and Micromodules,* the MEK6800D1 and MEK6800D2 Evaluation Kits, and other industry standard cards. This module provides 8192 bytes of storage and features full 16-bit address decoding with fully buffered data, address and control lines.

HIGH SPEED (480 ns max. access time)
LOW POWER (10 watts max.)
LOW DATA HOLD TIME (10 ns max.)
LOW BUS LOADING (0.36 mA max.)
SINGLE 5 VOLT POWER REQUIRED
SWITCH SELECTABLE OPERATING REGION

The 9626 is one of a family of M6800 Support Modules. The family provides building block hardware for data communication and industrial control systems and other systems that can benefit by the use of microprocessor techniques.

* Trade Mark of Motorola, Inc.

SERIES 96
SUPPORT MODULE
8192 BYTE STATIC
RANDOM ACCESS
MEMORY

ORDERING INFORMATION

8K MODULE	9626
KIT OF PARTS	9626K
UNPOPULATED CARD	9626-0

PHYSICAL CHARACTERISTICS:

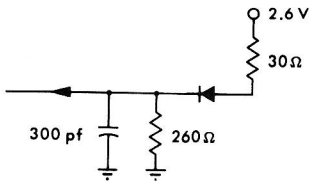
Overall Dimensions: 9.75 X 6.05 X 0.60 Inches (24.77 X 15.37 X 1.52 Cm.)

Edge Connector: 6.800 X 0.063 Inches (17.27 X 0.16 Cm.)

Board material, FR4 1/1

Finish: General, green epoxy solder mask both sides
Exposed pads, 70 microinches leveled solder (9626-0 only)
Edge connector, 50 microinches gold over nickel flash

Test load, D0-D7
Read Cycle Characteristics



ABSOLUTE MAXIMUM RATINGS (Voltage Referred to Ground Pin 43)

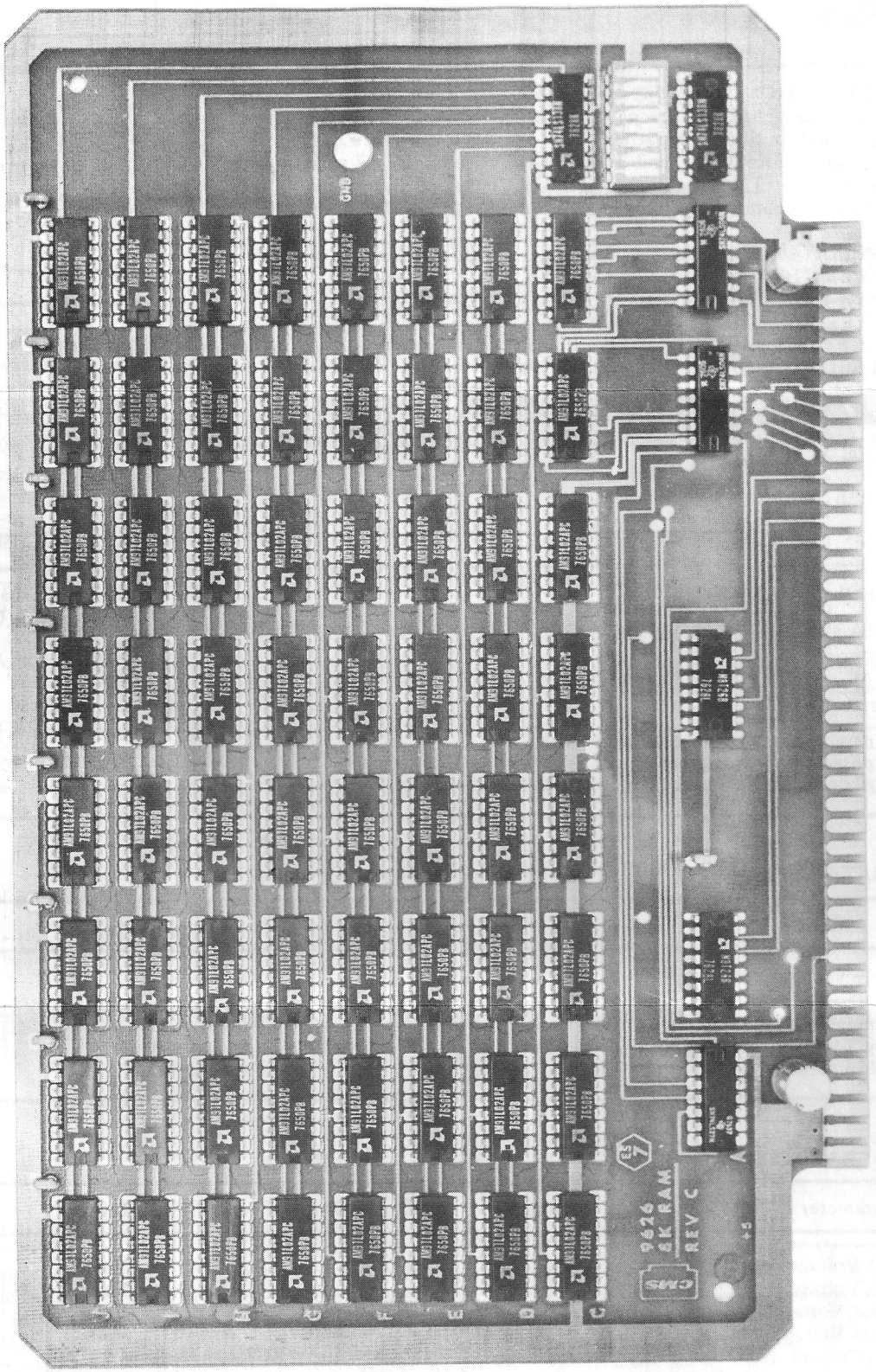
Rating	Symbol	Value	Units
DC Supply Voltage (Note 1)	V_{CC}	− 0.5 to + 7.0	VDC
Input Voltage, D0-D7	V_{DIN}	− 0.5 to + 5.5	VDC
Input Voltage, All Others	V_{IN}	− 0.5 to + 7.0	VDC
Operating Temperature Range	T_A	0 to + 70	Deg C
Storage Temperature Range	T_{STG}	− 40 to + 150	Deg C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = 0 to 70 Deg C)

Parameter	Conditions	Min.	Typ.	Max.	Units	Comments
Logical 1 Input Voltage V_{IH}		2.0			Volts	
Logical 0 Input Voltage V_{IL}				0.8	Volts	
Logical 1 Output Voltage V_{OH}	I_{OH} = − 10 mA	2.6	3.1		Volts	
Logical 0 Output Voltage V_{OL}	I_{OL} = 40 mA		0.25	0.5	Volts	
Logical 1 Input Current I_{IH}	V_{IH} = 2.7 V			25	uA	
Logical 0 Input Current I_{DIL}	V_{IL} = 0.4 V			-- 200	uA	D0-D7 Only
Logical 0 Input Current I_{IL}	V_{IL} = 0.4 V			-- 360	uA	Remaining Inputs
Input Clamp Voltage V_I	I_{IN} = − 5 mA			-- 1.0	Volts	
Short Circuit Output Current I_{OS}	V_O = 0 V	-- 50		-- 150	mA	Note 2
Power Supply Current I_{CC}			1.5	2.0	Amp	

Notes: 1. Maximum duration above 5.5 V, 1 Second
2. One output at a time
3. This preliminary information is subject to change without notice.

9626



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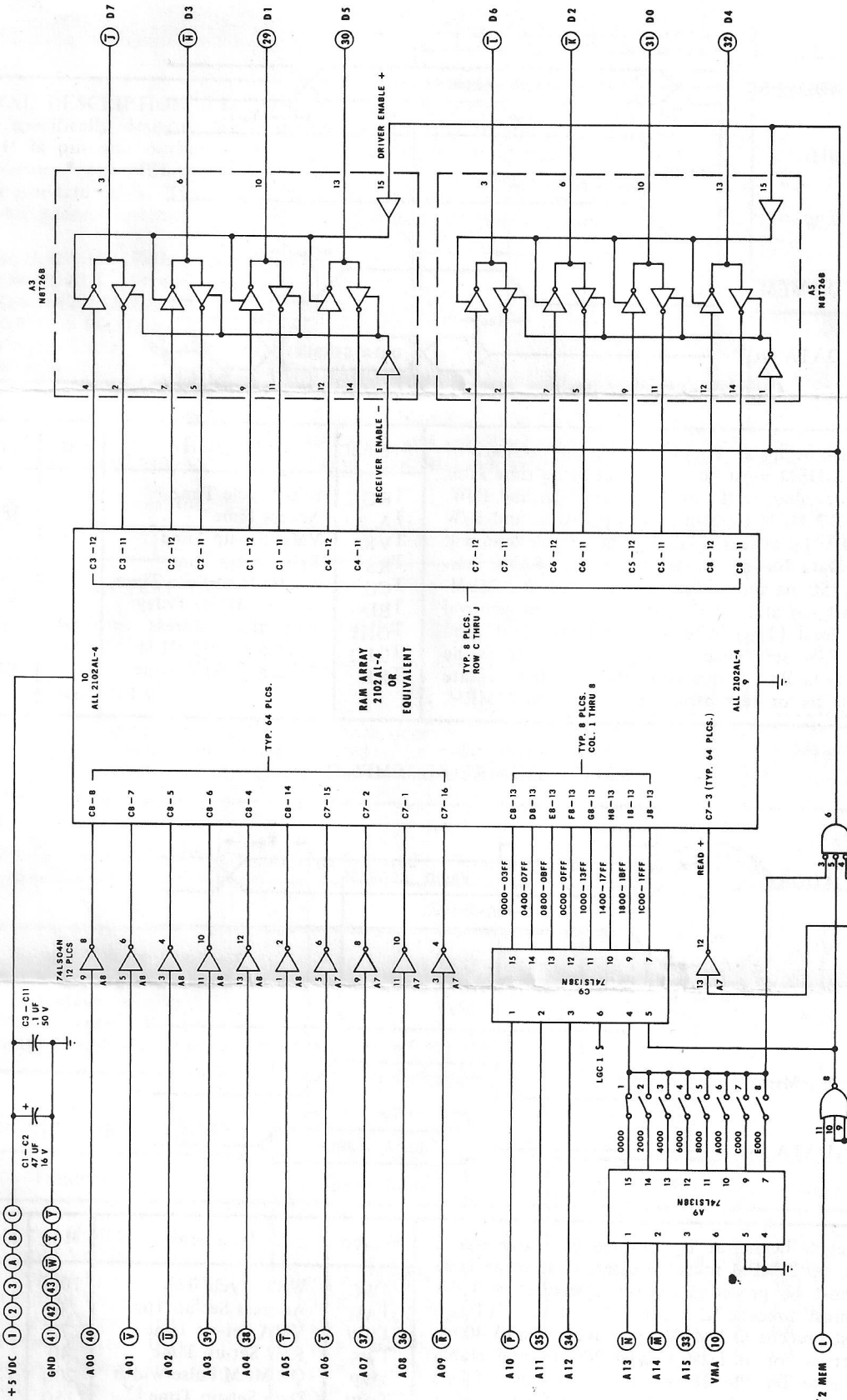

Schematic Diagram
9626 Rev. C

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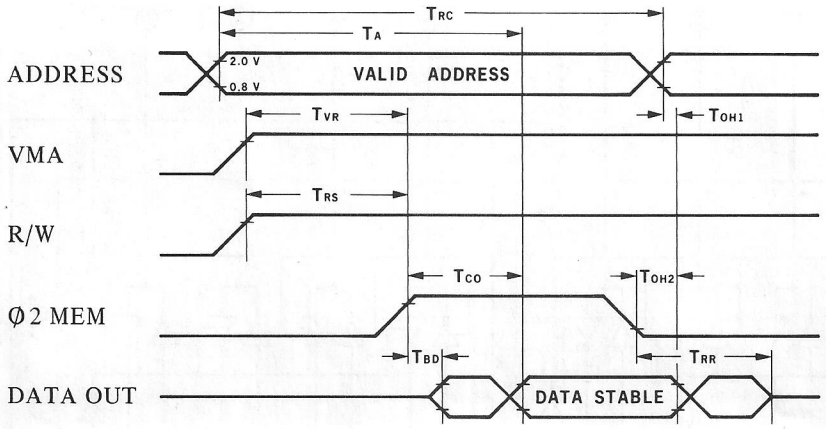
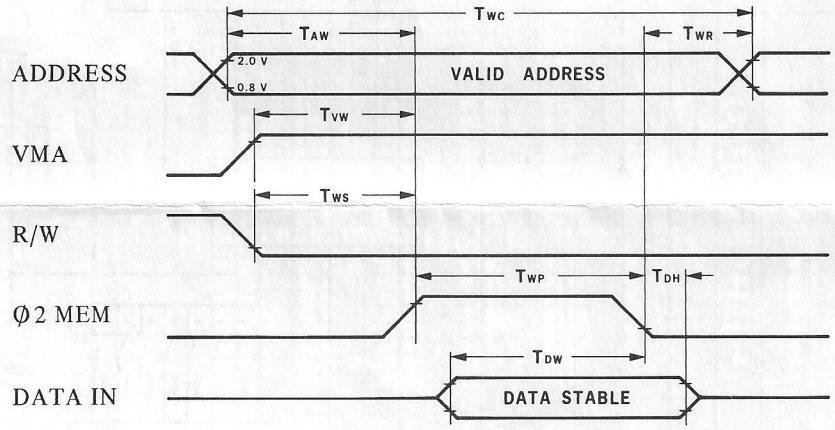
READ CYCLE CHARACTERISTICS



The normal read cycle begins at T_0, defined by the presence of a stable address. Ø2 MEM must be asserted at some time after T_0 and it must be preceded by the assertion of VMA and R/W. VMA must precede Ø2 MEM by at least (T_{VR}) 70 ns and R/W must precede Ø2 MEM by at least (T_{RS}) 40 ns. Stable data will be available on the Data Bus at the latter of (T_A) 480 ns max. after T_0 or (T_{CO}) 250 ns max. after assertion of Ø2 MEM. Valid data will persist for at least (T_{OH2}) 30 ns after removal of Ø2 MEM or at least (T_{OH1}) 80 ns after removal of valid address. VMA and R/W are expected to persist as long as the valid address. The Data Bus drivers will return to the tri-state condition (T_{RR}) 80 ns or less after removal of Ø2 MEM.

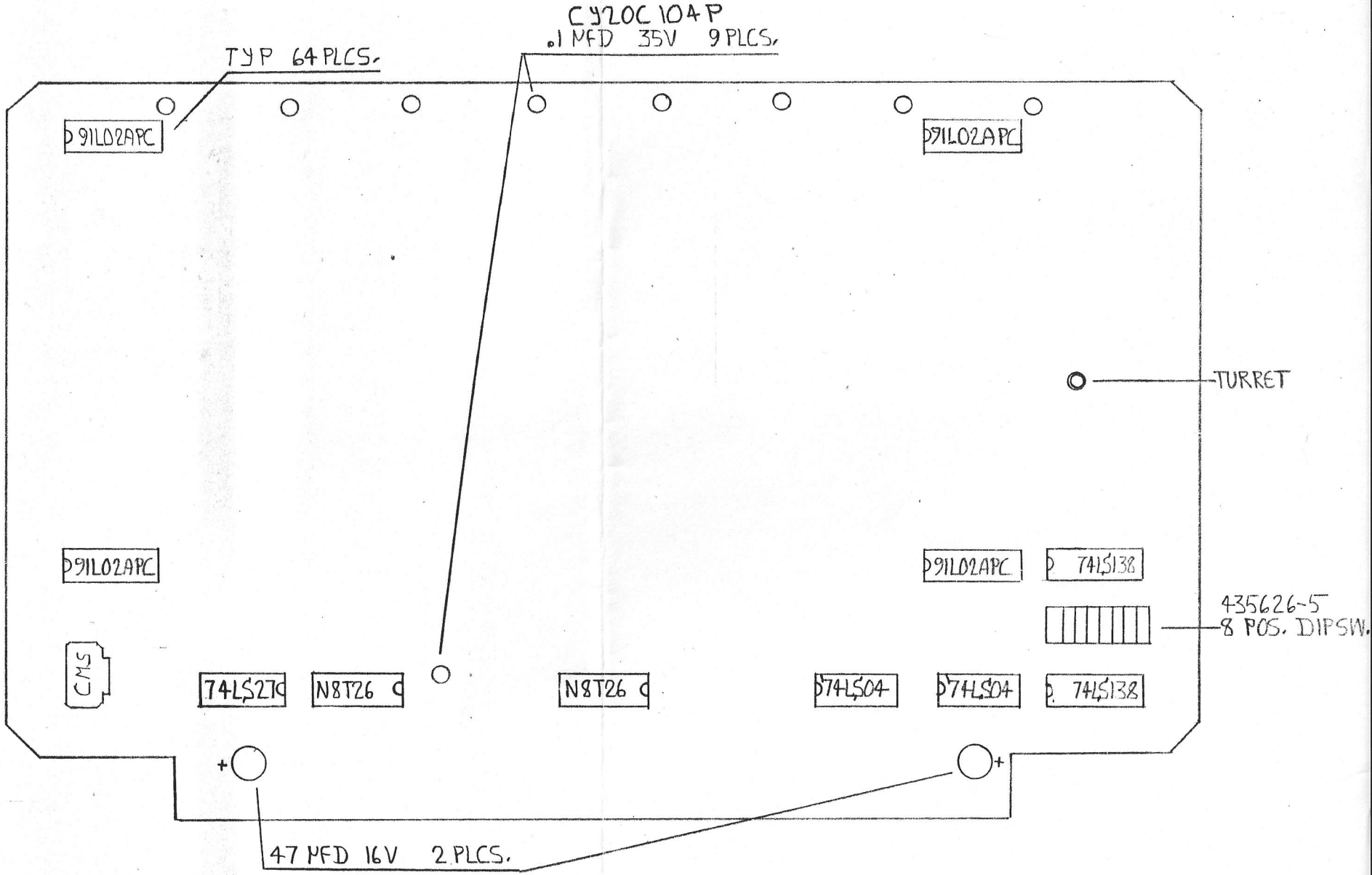
Symbol	Parameter	Min.	Max.	Units
T_{RC}	Read Cycle Time	1000		ns
T_A	Access Time		480	ns
T_{VR}	VMA Set-up Time	70		ns
T_{RS}	R/W Set-up Time	40		ns
T_{CO}	Ø2 MEM to Data Time		250	ns
T_{BD}	HI Z to Active Delay		80	ns
T_{OH1}	Valid after Address	80		ns
T_{OH2}	Valid after Ø2 MEM	30		ns
T_{RR}	Return to HI Z Time		80	ns

WRITE CYCLE REQUIREMENTS



The normal write cycle begins at T_0, defined by the presence of a stable address. Ø2 MEM must be asserted at some time after T_0 and it must be preceded by the assertion of VMA and R/W. VMA must precede Ø2 MEM by at least (T_{VW}) 70 ns and R/W must precede Ø2 MEM by at least (T_{WS}) 40 ns. Ø2 MEM must persist for at least (T_{WP}) 200 ns and stable data must be available on the Data Bus for at least (T_{DW}) 150 ns before its removal and for at least (T_{DH}) 10 ns after its removal. The valid address must persist for at least (T_{WR}) 25 ns after removal of Ø2 MEM.

Symbol	Parameter	Min.	Max.	Units
T_{WC}	Write Cycle Time	1000		ns
T_{AW}	Address Set-up Time	0		ns
T_{VW}	VMA Set-up Time	70		ns
T_{WS}	R/W Set-up Time	40		ns
T_{WP}	Ø2 MEM Pulse Width	200	2500	ns
T_{DW}	Data Set-up Time	150		ns
T_{DH}	Data Hold Time	10		ns
T_{WR}	Write Recovery Time	25		ns



9626 REV C COMPONENT PLACEMENT